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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/812,395	03/30/2004	Jens Egerer	QIM 2003 P 50294 US	1743

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EXAMINER	
RUTLAND WALLIS, MICHAEL	
ART UNIT	**PAPER NUMBER**
2836	

MAIL DATE	DELIVERY MODE
11/13/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

TH

Office Action Summary	Application No.	Applicant(s)	
	10/812,395	EGERER, JENS	
	Examiner	Art Unit	
	Michael Rutland-Wallis	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 October 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21,23 and 27-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21,23 and 27-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 10/09/2007 has been entered.

Claim Objections

Claim 23 recites the limitation "first and second operating modes". There is insufficient antecedent basis for this limitation in the claim. Applicant should amend claim 23 consistent with the amended mode language currently present in claim 1.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -
(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claims 1, 8, 18 and 23 are rejected under 35 U.S.C. 102(b) as being anticipated by Matsumoto et al. (U.S. Pub. No. 20050189566)

With respect to claims 1, 8, 18 and 23 Matsumoto teaches a system comprising: a first semiconductor device (item 2A), and a second semiconductor device (item 2B), wherein the first semiconductor device and the second semiconductor device each comprise a voltage supply device (items P_A and P_B see paragraph 0043), wherein said voltage supply device (P_A) of said first semiconductor device (2A) is connected to said second semiconductor device (2B), so that said voltage supply device of said first semiconductor device can provide a supply voltage (via leg portion item 8 or 12 for example see paragraph 0039) for said second semiconductor device (2B), and wherein the system is adapted such that, in an external access operating mode (normal operations mode) of the second semiconductor device (2B), the voltage supply device of said second semiconductor device provides the supply voltage for the second semiconductor device, and, in a standby or refresh operating mode (power-save mode see paragraph 0039) of the second semiconductor device, the voltage supply device of said first semiconductor device provides the supply voltage for the second semiconductor device (see paragraph 0039 where Matsumoto teaches one the semiconductors is put into a non-operating mode).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2-7, 9-11, 19-21, and 27-31 rejected under 35 U.S.C. 103(a) as being unpatentable over Matsumoto et al. (U.S. Pub. No. 20050189566)

With respect to claims 2 and 3 Matsumoto does disclose a housing. Matsumoto however does arrange the semiconductors in a stacked manner (see Fig. 5 for example). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Matsumoto to include a housing for the stacked semiconductors in order to protect the devices from outside damage.

With respect to claim 4-7 Matsumoto teaches the boards are plug mountable (see Fig. 5C) however Matsumoto does not teach the housing is a plug mountable device housing. Applicant admits in page 2 lines 24-31 of the disclosure semiconductors are usually incorporated in appropriate housings e.g. SMD, plug mountable, DIL, PGA etc... It would have been obvious to one of ordinary skill in the art at the time of the invention to connected semiconductors as appropriate to the housing in order to provide a simple and reliable connection to other connected semiconductors.

With respect to claim 9 Matsumoto teaches said one further semiconductor device may be arranged in the stack, as the first and said second

semiconductor devices (2A and 2B). Matsumoto does not teach the circuitry is contained within a housing, semiconductor components are typically found in a housing and not exposed. It would have been obvious to one of ordinary skill in the art at the time of the invention to put the stack of Matsumoto into a housing if in fact such a housing is not utilized by Matsumoto in order to protect the semiconductor.

With respect to claims 10 and 11 Matsumoto teaches said voltage supply of said first semiconductor device (2A) is additionally also connected to said one or to said several further semiconductor device (see paragraph 0076), so that said voltage supply of said first semiconductor device (2A) can additionally provide a supply voltage for said one or said several further semiconductor device(s).

With respect to claim 19 Matsumoto teaches the power supplied comprises regulators or converters.

With respect to claims 20 and 21 Matsumoto teaches the voltage supply means comprise a voltage regulating means and charge pump to control the voltage to the modules with different voltage requirements.

With respect to claim 27 Matsumoto teaches the use of electronic components and external control to select a second mode of power savings, however does not illustrate the use of a fuse. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Matsumoto to use a fuse to carry out the control mode selection of the first and second semiconductor devices.

With respect to claim 28-31 Matsumoto teaches wherein said voltage supply means of said first semiconductor device is connected to a corresponding pad of said first semiconductor device (See Fig. 5C).

Claims 12-17 and 32-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsumoto et al. (U.S. Pub. No. 20050189566) in view of Odisho et al. (U.S. Pat. No. 5,758,100)

With respect to claim 12-14 and 32-33 Matsumoto is silent on the on the detailed nature of the components specifically whether the first semiconductor device is a memory device. Odisho teaches a typical semiconductor integrated circuit (item 202) comprising a memory device (RAM module item 212). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the semiconductor voltage supply configuration of Matsumoto with memory devices as seen in Odisho in order to supply memory modules with variable voltage requirements.

With respect to claim 15 Matsumoto as modified by Odisho are silent on whether the RAM is DRAM (dynamic RAM) as understood by the examiner the RAM modules are DRAM modules, while not explicitly stated by Odisho, however should one content otherwise, It would have been obvious to one of ordinary skill in the art at the time of the invention to use DRAM modules in order to supply typical memory modules is a computer with voltage.

With respect to claim 16 Odisho teaches the memory devices items 212 and additional circuitry may comprise a graphics card or a network card (col. 2 line 55) know to one of ordinary skill in the art to utilize ROM.

With respect to claim 17 Matsumoto as modified by Odisho teach said memory device is a functional memory device or fundamental memory devices, respectively, in particular PLDs and/or PLAs as the memory devices of Odisho are controlled by a memory address bus and made up of transistors.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael Rutland-Wallis whose telephone number is 571-272-5921. The examiner can normally be reached on Monday-Thursday 7:30AM-6:00PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Sherry can be reached on 571-272-2084. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

11/8/02

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